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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,297	07/11/2003	Nobuyoshi Osamura	11-170	2917

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,297	OSAMURA ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20-28* is/are pending in the application.

4a) Of the above claim(s) *6,7,12 and 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8,20-22 and 26-28* is/are rejected.

7)☒ Claim(s) *2-5,9-11,13,14,16-18 and 23-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 3/17/05 has been received and entered in the case. The amendment and argument presented therein overcome the informality objections, and therefore, these are withdrawn. New grounds of rejections necessitated by the amendment are needed as set forth below. This action is FINAL.

Claim Objections

2. Claims 21 and 27 are objected to because of the following informalities:

In claim 21, line 2, "the first and second" should be changed to -- the input and output --, see line 3 of claim 1,

In claim 27, line 2, the same problem exists as discussed in claim 21.

Appropriate correction is required.

Double Patenting

3. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claim 18 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 16. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 8, 20, 22 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,201,674, issued to Warita et al.

As per claim 1, Warita discloses a power supply circuit (figure 1), comprising:

an electric switching element (transistor TR) placed in a power transmission path connecting an input terminal (P1) and an output terminal (P2) and a load connected to the output terminal (the load is the circuit which is connected to the output terminal P2, powered by the power supply circuit, not shown);

a voltage detecting circuit (voltage divider, R31 and R32) detecting the output voltage (VO) supplied through the output terminal;

a reference-voltage producing circuit (17) producing a reference voltage (VREF1) in accordance with a target voltage (a predetermined voltage set by the user);

a voltage control circuit (op-amp 16) controlling the switching element TR so that the detected output voltage tracks the reference voltage (the output of the comparator 16 provides the control signal to the base of Q12 to turn ON/OFF transistor TR by controlling the base current of transistor TR);

a current detecting circuit (resistor RP) detecting an output current supplied through the output terminal (by sensing the voltage drop across resistor RP);

a limited-current-value setting circuit (op-amp 18) setting a limited value to the output current (the comparator 18 detects the output current IO, when the output current IO is greater than a predetermined value, transistor Q10 is ON to limit the output current), wherein the limited value increases gradually over time during a rise of the output voltage up to the target voltage (during a rise of the output voltage up to the target voltage, the output voltage at the op-amp 18 is gradually increased); and

a current limiting circuit (transistor Q10) controlling the switching element to keep the detected output current at a value less than or equal to the limited value during the rise of the output voltage to the target voltage (transistor Q10 controls the base current of transistor Q12, and therefore, the base current of TR is controlled), the current limiting control having priority over an output voltage tracking control (because Q10 controls the base current of transistor Q12).

As per claim 8, the recited limitation is disclosed in column 7, lines 9-10.

As per claim 20, as shown, TR is a transistor.

As per claim 22, this claim is rejected for the same reasons noted in claim 1. Further, the recited "predetermined delay time" reads on the time the application is started to apply to the input terminal to the time the output voltage is up to the target value.

As per claim 26, this claim is rejected for the same reason noted in claim 20.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,201,674, issued to Warita et al. in view of the applicant's admitted prior art.

As per claim 21, Warita discloses a power supply circuit having the structure as discussed in claim 1 wherein the reference-voltage producing circuit, the voltage control circuit, the limited-current-value setting circuit, and the current limiting circuit are formed into an integrated circuit IC 12.

Warita does not explicitly disclose the circuit further comprises first and second smoothing circuits and the voltage detecting circuit is formed into an integrated circuit as called for in the claim.

The applicant's admitted prior art (figure 1) discloses first (capacitor C1) and second (capacitor C2) smoothing circuits connected to the input and output terminals, respectively, and the voltage detecting circuit is formed into an integrated circuit.

It would have been obvious to one skilled in the art at the time of the invention was made to include the first and second smoothing circuits connected to the input and output terminals of the Warita's power supply circuit. The motivation and/or suggestion would be to reduce the

noise components of the input signal and output signal of the Warita's power supply circuit so that the Warita's power supply circuit can be used in an application which requires a clean power.

Further, it would have been obvious to one skilled in the art at the time of the invention was made to include the Warita's voltage detecting circuit in the integrated circuit IC 12 as well. The motivation and/or suggestion would be to increase the reliability of the Warita's power supply circuit because when discrete components of a circuit are integrated into a chip, the circuit is more reliable.

As per claims 27-28, these claims are rejected for the same reasons noted in claim 21.

Response to Arguments

6. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

7. Claims 2-5, 9-11, 13-14, 16-18 and 23-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-5 are allowable because the prior art of record fails to disclose or suggest the inclusion of a limited current value setting circuit which is configured to stepwise increase the limited value to the output current as time progresses as recited in claim 2.

Claims 9-11, 13-14 and 16-18 are allowable because the prior art of record fails to disclose or suggest the inclusion of a control delay circuit as recited in claim 9.

Claims 23-25 are allowable for the same reason noted in claim 9.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/23/05

Minh Nguyen
Primary Examiner
Art Unit 2816